ABSTRACT

A current summing FIR filter can be implemented with multiple differential input stages and variable tail currents. The variable tail currents can be used to appropriately weight the present and previous digital input signals. The weighted outputs of the differential transistor pairs can be summed to provide a filtered output signal. The tail currents can be advantageously varied with variable current sources or by adjustment of the relative widths of the differential transistor pairs. In other embodiments, additional differential pairs can be added to adjust for systematic offset voltages caused by process-induced variations in the structure of circuit devices or to induce a desired offset.

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